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a VHDL module in Verilog 90, and am using the multiple ports API, but one of the properties of the port entity keeps giving a "cannot assign "-1" to "VHDL\_SIGNAL". If I run my code with a simulator, it works, but when I compile it and try to simulate it, it fails. Here is my code:

```
entity my_entity is generic(
vs_managed : STD_LOGIC := '0' ); port (
clk, reset : in std_logic; vs, vd : in
std_logic; o : out std_logic ); end entity
my_entity; architecture Behavioral of
my_entity is signal o_sig : std_logic;
begin process(clk, reset) begin if reset =
'1' then o
```

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